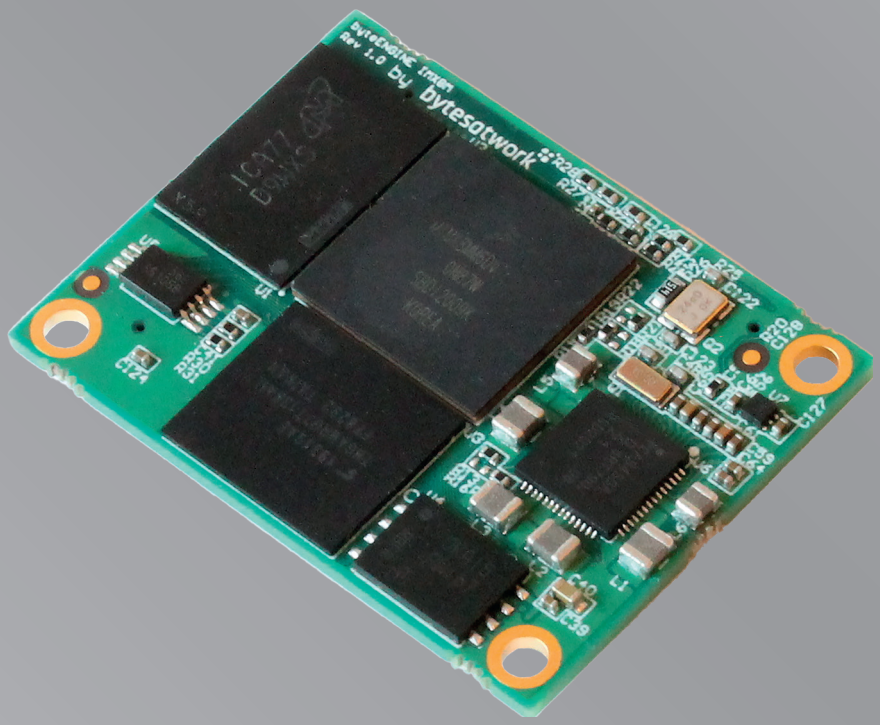
DataSheet

industrial computing module

byteENGINE IMX8MM

12.07.2023



bytesatwork

Copyright notice

Copyright 2021 bytes at work AG, CH-8406 Winterthur,
Switzerland. All rights reserved.

Reproduction in any form or by any means without permission is prohibited. bytes at work reserves the right to make improvements to the products described in this manual at any time without notice.

No part of this manual may be reproduced, copied, translated, or transmitted in any form or by any means without the prior written permission of the company. Information provided in this manual is intended to be accurate and reliable. However, bytes at work assumes no responsibility for its use, or for any infringements upon the rights of third parties that may result from its use.

The material in this document is for product information only and is subject to change without notice. While reasonable efforts have been made in the preparation of this document to assure its accuracy, bytes at work assumes no liabilities resulting from errors or omissions in this document, or from the use of the information contained herein. bytes at work reserves the right to make changes in the product design without notice to its users.

Trademarks

Product names, logos, brands, and other trademarks featured,
or referred to are the property of their respective trademark holders.
These include, but are not limited to uboot, Linux and ARM.

Disclaimer

Bytes at work AG does not guarantee that the information in this manual is up-to-date, correct, complete or of good quality. Nor does bytes at work AG assume guarantee for further usage of the information. Liability claims against bytes at work AG, referring to material or non-material related damages caused, due to usage or non-usage of the information given in the manual, or due to usage of erroneous or incomplete information, are exempted, as long as there is no proven intentional or negligent fault of bytes at work AG.
Bytes at work AG explicitly reserves the rights to change or add to the contents of this manual or parts of it without special notification.

Imprint

> bytes at work AG
Technoparkstrasse 7
CH-8406 Winterthur
+41 52 213 79 79

> info@bytesatwork.ch
www.bytesatwork.io

Symbols and typographic conventions

These symbols represent important details or aspects for working with bytes at work AG-products.

NOTICE
Follow instructions. Acting against the procedure described can lead to malfunction.

LINK
Hyperlink or link to chapter.

1. Table of Contents

2. Revisions History

Hardware Revision	Marking on PCB	Release Date	Note
1.1	Rev 1.1	2021	First revision for sale

3. Overview

3.1 General Information

The i.MX 8M Mini applications processor represents NXP's latest video and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption. The i.MX 8M Mini family of processors features advanced implementation of a quad Arm® Cortex®-A53 core, which operates at speeds of up to 1.8 GHz. A general purpose Cortex®-M4 400 MHz core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3L memory. A wide range of audio interfaces are available, including I2S, AC97, TDM, and S/PDIF. There are a number of other interfaces for connecting peripherals, such as USB, PCIe, and Ethernet.

3.2 Technical Data

Feature		Details
CPU	Architecture	up to Quad symmetric Cortex-A53 processors
	CPU	i.MX 8M Mini See LINK for further information: „3.4 Additional information" See NXP Homepage for further information: i.MX 8M Mini
	Cache	• 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • 512 kB unified L2 Cache
	Frequency (max)	1.6 / 1.8 GHz
	Floating Point	Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
	Co Processor	Cortex®-M4 400 MHz core processor for low-power processing • 16 kB L1-I Cache/ 16 kB L1-D Cache
	Security	Arm Cortex-A53 TrustZone
GPU		3D: GCNanoUltra (1x shader, OpenGL® ES 2.0) 2D: GC320

©bytes at work

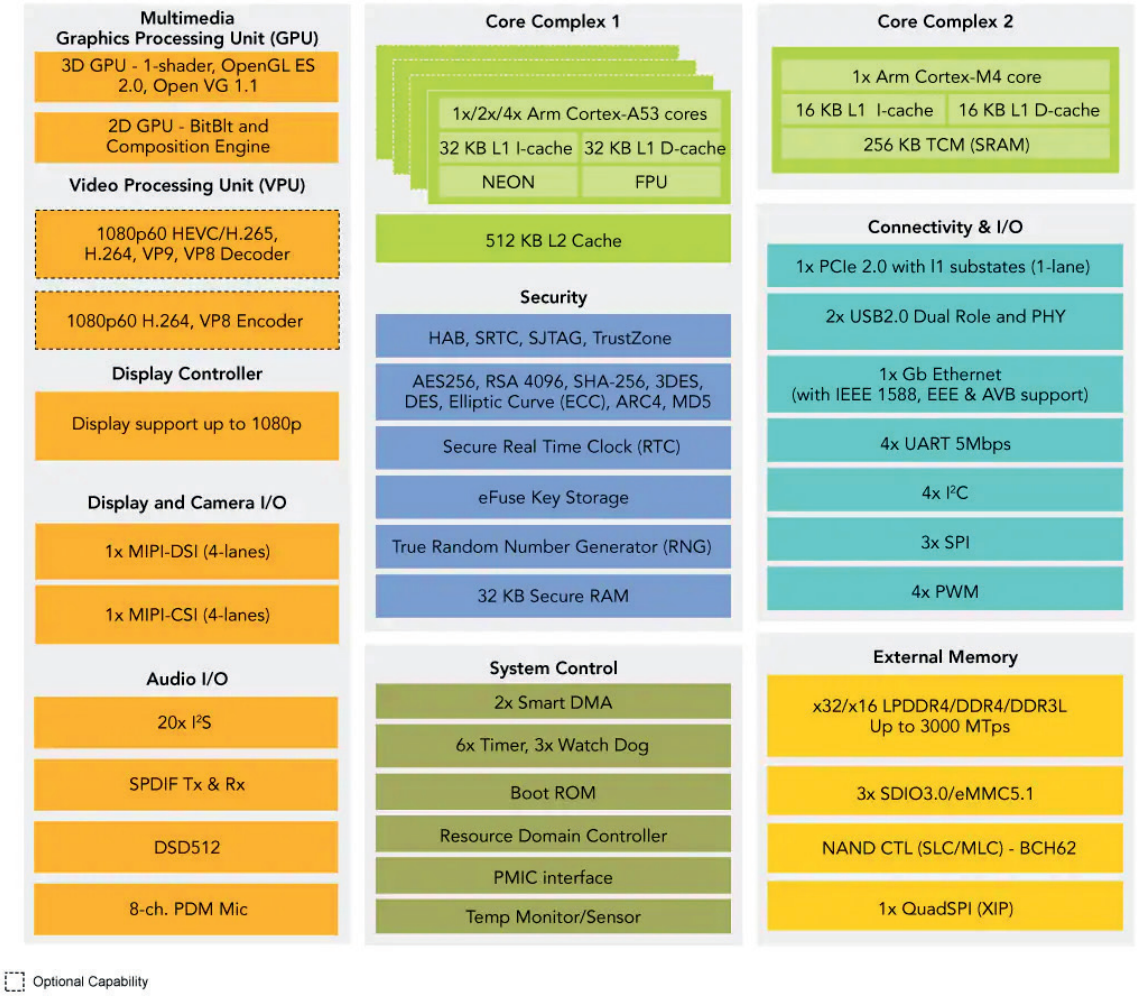
Feature		Details
Memory on Chip	Boot ROM	256 KB
	RAM	256 KB + 32 KB
Memory External	DRAM	up to 4 GB LPDDR4
	FLASH	up to 64 GB eMMC 8 MB QSPI NOR
	EEPROM	32 kB EEPROM
Ethernet	Speed	1 x 10/100/1000 Mbps & IEEE 1588
Multimedia	Video Processing Unit	• 1080p60 VP9 Profile 0, 2 (10-bit) • 1080p60 HEVC/H.265 Decoder • 1080p60 AVC/H.264 Baseline, Main, High decoder • 1080p60 VP8 • 1080p60 AVC/H.264 Encoder • 1080p60 VP8
	Graphic Processing Unit	• GCNanoUltra for 3D acceleration • GC320 for 2D acceleration
	LCDIF Display Controller	• Supports up to 2 layers of overlay • Supports up to 1080p60 display through MIPI DSI
	Audio	• S/PDIF input and output, including a new Raw Capture input mode • Five synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces, including one SAI with 8 Tx and 8 Rx lanes, one SAI with 4 Tx and 4 Rx lanes, two SAI with 2 Tx and 2 Rx lanes, and one SAI with 1 Tx and 1Rx lane. Supports over 20 channels of audio subject to I/O limitations. • 8-Channel Pulse Density Modulation (PDM) input
Expansion	SD/SDIO, MMC, SDXC	3 x (HS400, SDIO 3.0)
Serial	SPI	3
	I2C	4
	UART	4
	SPI	3
	PCI Express (PCIe Gen2, single lane)	1
USB		2 x USB 2.0 OTG
Miscellaneous	Watchdog	3
	JTAG	Yes
	GPIO (5 * 32 Bit)	160 GPIOS
	PWM	4
	Timer	6
	Boot Mode	High Assurance Boot (HAB)
	RTC	Secure real-time clock
Mechanical Information	Input Voltage	5 .0 V
	Power Consumption	4 W
	Dimensions	30 x 40 mm
	Operating Temperature	• Industrial temperature range: -40 to +85° C • Consumer temperature range: 0 to 95° C
	Connector	2x 100 pin
Operating System	Linux	meta-bytesatwork available on github

3.3 Block diagram of i.MX 8M Mini

The i.MX 8M Mini is NXP's first embedded multicore applications processor built using advanced 14LPC FinFET process technology, providing more speed and improved power efficiency. With commercial and industrial level qualification and backed by NXP's product longevity program, the i.MX 8M Mini family may be used in any general purpose industrial and IoT application.

Key Features of i.MX 8M Mini

- Quad Arm® Cortex®-A53 core, up to 1.8 GHz.
- Cortex®-M4 400 MHz processor
- VIVANTE GC NANO Ultra 3D GPU
- VIANVTE GC 320 2D GPU
- Video processing unit
- Trust zone support



3.4 Additional information

For further information regarding the i.MX 8M Mini CPU, please visit the homepage of NXP.

LINK:
NXP i.MX 8M Mini

3.5 Decision guidance byteENGINE IMX8MM

The following four steps help you identify the suitable processor for the specific customer application.

> Step 1: Select the needed CPU.

  > **Choose Quad/Quad Lite or Dual A53 Cortex**
  For details see „3.2 Technical Data“

> Step 2: Select the needed flash memory type and capacity.

  > **Choose eMMC 8 / 16 / 32 / 64 GB**

> Step 3: Select the needed RAM capacity.

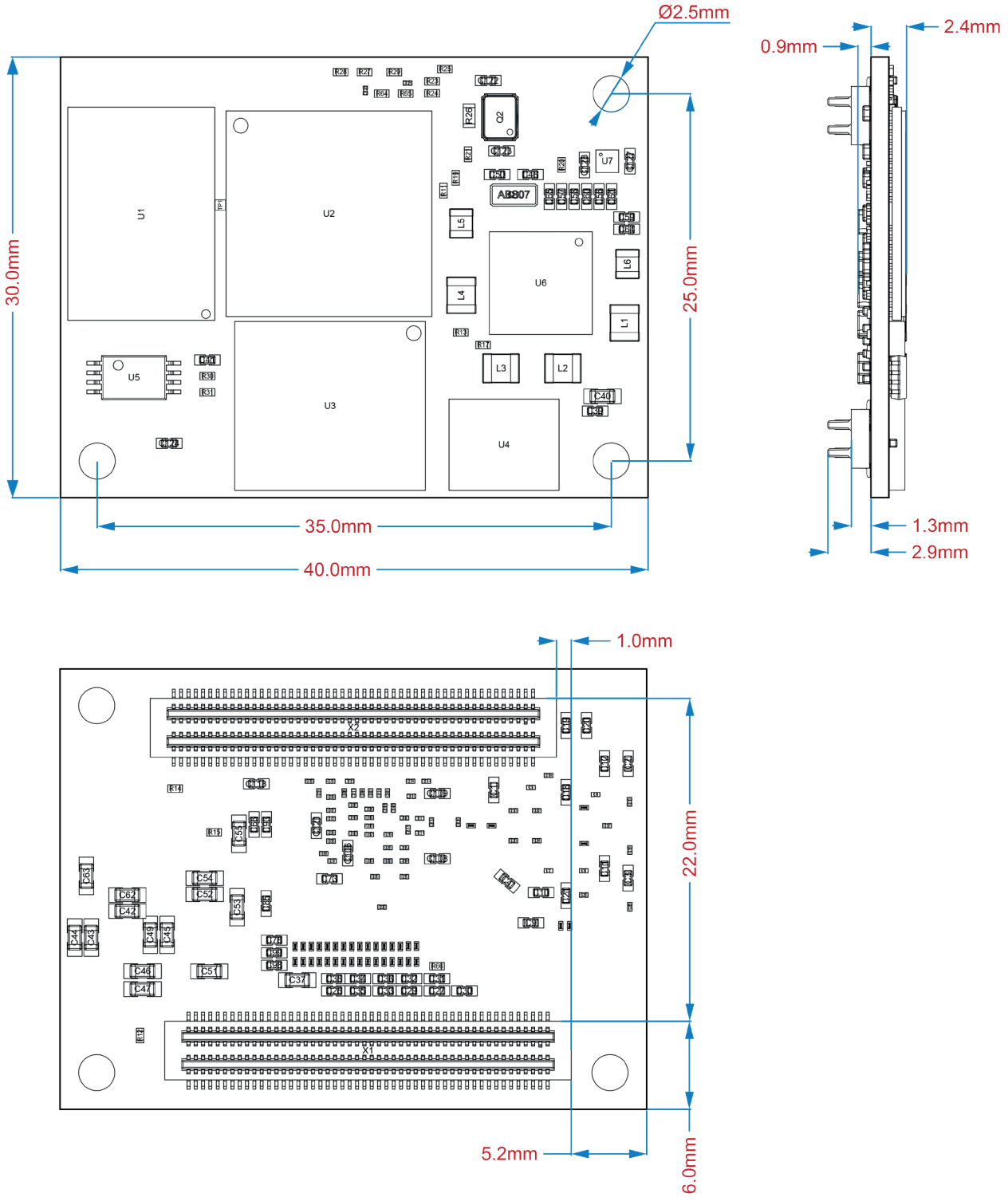
  > **Choose 512 / 1024 / 1536 / 2048 / 4069 MB**

> Step 4: Select the the needed temperature range.

  > **Choose consumer or industrial**

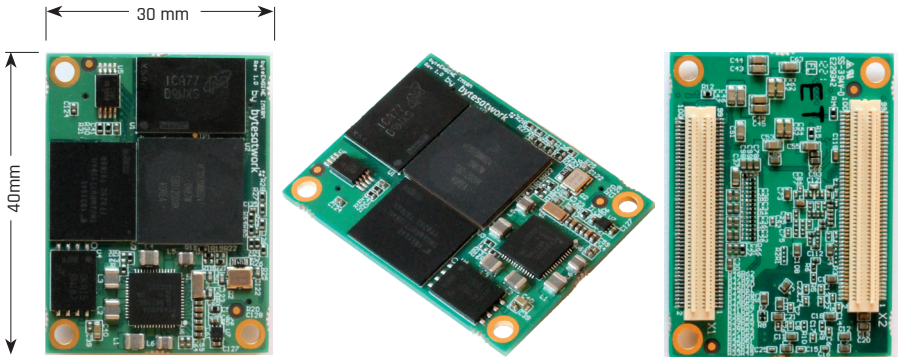
3.6 Dimensions of byteENGINE IMX8MM

The following illustration shows all important dimensions for mounting and installation of the industrial computing module byteENGINE IMX8MM.



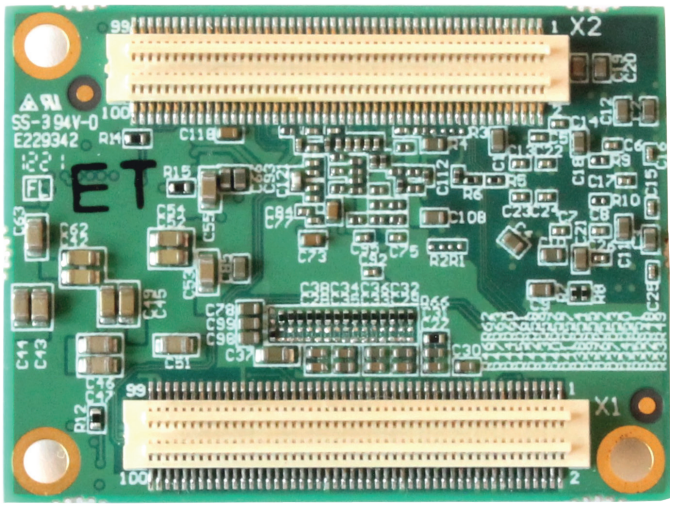
©bytes at work

> Module design in scale 1:1:



3.7 byteENGINE IMX8MM connectors layout

The byteENGINE IMX8MM is connected to the carrier board with 200 pins on two module connectors.
The following picture shows the location of the connectors on the bottom side of the SOM byteENGINE.



CONNECTORS

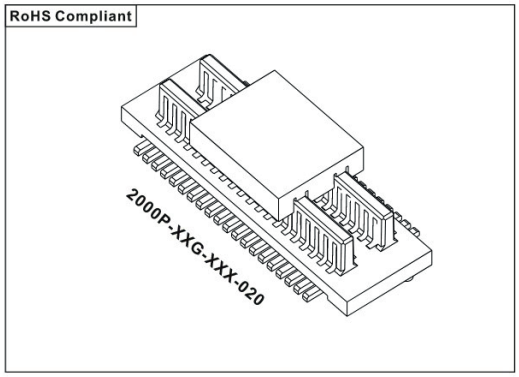
X1	SPDIF, I2C, USB, Ethernet, SPI, SAI, MMC, JTAG
X2	Power, PWM, DSI, CSI, PCIE, SAI

LINK:
Schematic of the connectors X1 and X2

NOTICE
The module is held in the connectors with a considerable retention force. To avoid damaging the modules' connectors as well as the carrier board connectors while removing the module the use of an extraction tool is strongly recommended.

3.8 Connectors - Neltron 2001S-100G-270-020

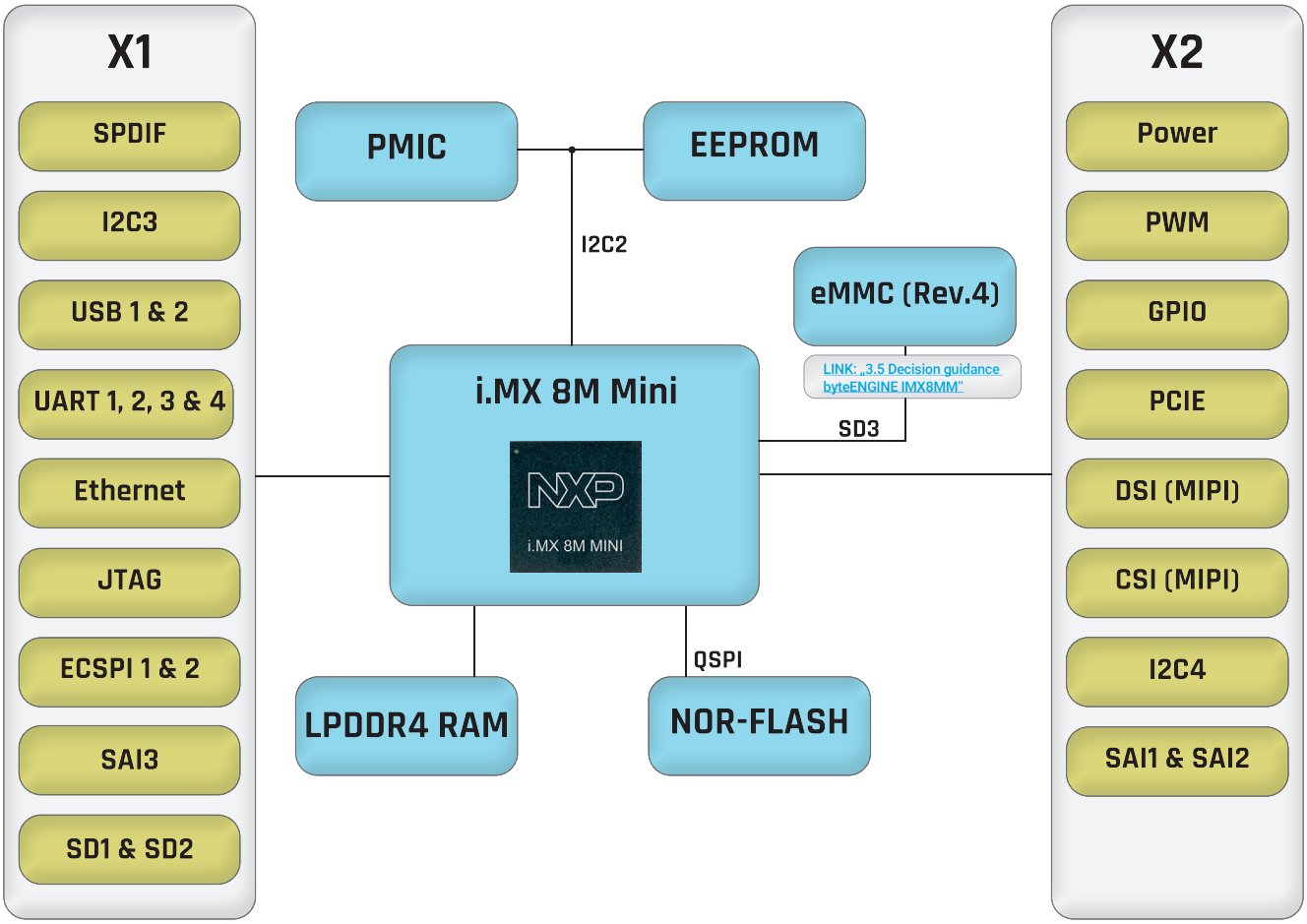
The byteENGINE uses two Neltron 0,5mm Board to Board Plug connectors.
For more specific information about the connectors used, please visit:



LINK:
Datasheet of Neltron 0.5 mm connectors

3.9 byteENGINE IMX8MM Connectors Overview

The following illustration shows the „default configuration“ of the byteENGINE IMX8MM. The function of the components shown in blue squares cannot be changed. The yellow squares show the module connectors X1 and X2. The functions of X1 and X2 can be adapted and each connector module serves multiple functions. The detailed pinout functions are shown in chapter **„4. Pinout“**.



3.10 Configuration tool for I.MX processors

The **Config Tools for i.MX** is a suite of evaluation and configuration tools that help users from initial evaluation to production software development. Config Tools for i.MX is an easy-to-use way to configure the pins and DDR of the i.MX processor devices.

The Config Tools for i.MX is installed as a desktop tool which then loads additional device information through a network connection, but does otherwise not need internet connection. It does not require a project setup, as all the settings are stored in text and generated source files, which then can be easily stored in a version control system or exchanged with other users.

The Pins Tool makes pin configuration easier and faster with an intuitive and easy user interface, which then generates normal C code that can then be used in any C and C++ application. The Pins Tool configures pin signals from multiplexing (muxing) to the electrical properties of pins, and it also creates Device Tree Snippets Include (.dtsi) files and reports in CSV format.

The DDR tool provides two main functionalities: configuration and validation. The DDR configuration provides a user-friendly graphical interface to configure the DDR controller and the DDR PHY. It can be used for tweaking some of the configuration parameters when you want to use different memory modules than the ones received with the board or when you want to optimize the configuration. DDR validation provides different scenarios to verify the DDR performance, by downloads a test image to the processor's internal RAM through a USB connection. The result is sent to the DDR tool via the UART. DDR validation can help verify DDR stability on the board in a non-OS environment.

NOTICE
Follow the link to i.MX Config Tool below. You need to install the Tool. Then choose the processor.

LINK:
NXP Config Tools for i.MX Applications Processors

LINK:
byteENGINE IMX8MM Config File for Config Tools

4. Pinout

4.1 Restrictions

These peripherals are internally connected and should not be utilized in the customer design if the components are populated and in use.

Restricted peripherals

I2C2	PMIC and EEPROM
SD3	eMMC
QUADSPI	SPI NOR Flash
SAI1	Boot Mode

NOTICE
Caution when using the SAI1: Bootpins!

4.2 Carrier board connectors X1

X1: PIN 1 - 27

Con	Pin	Signal Name	GPIO Mode	Alternative Modes on Pin			
				1	2	3	4
X1	1	BOOT0		SRC_BOOT_MODE0			
X1	2	GND					
X1	3	SPDIF_EXT_CLK	GPIO5_IO05	PWM1_OUT	SPDIF1_EXT_CLK		
X1	4	I2C3_SCL	GPIO5_IO18	PWM4_OUT	GPT2_CLK	I2C3_SCL	
X1	5	SYS_NRST					
X1	6	I2C3_SDA	GPIO5_IO19	PWM3_OUT	GPT3_CLK	I2C3_SDA	
X1	7	SPDIF_TX	GPIO5_IO03	PWM3_OUT	SPDIF1_OUT		
X1	8	SPDIF_RX	GPIO5_IO04	PWM2_OUT	SPDIF1_IN		
X1	9	USB2_DN		USB2_DN			
X1	10	USB1_DN		USB1_DN			
X1	11	USB2_DP		USB2_DP			
X1	12	USB1_DP		USB1_DP			
X1	13	USB2_VBUS		USB2_VBUS			
X1	14	USB1_VBUS		USB1_VBUS			
X1	15	USB2_ID		USB2_ID			
X1	16	USB1_ID		USB1_ID			
X1	17	GND					
X1	18	GND					
X1	19	ENET_MDC	GPIO1_IO16	ENET1_MDC			
X1	20	ENET_MDIO	GPIO1_IO17	ENET1_MDIO			
X1	21	GND					
X1	22	GND					
X1	23	ENET_TD0	GPIO1_IO21	ENET1_RGMII_TD0			
X1	24	ENET_RD0	GPIO1_IO26	ENET1_RGMII_RD0			
X1	25	ENET_TD1	GPIO1_IO20	ENET1_RGMII_TD1			
X1	26	ENET_RD1	GPIO1_IO27	ENET1_RGMII_RD1			
X1	27	ENET_TD2	GPIO1_IO19	ENET1_RGMII_TD2	ENET1_TX_CLK	CCM_ENET_REF_CLK_ROOT	

©bytes at work

X1: PIN 28 - 73

Con	Pin	Signal Name	GPIO Mode	Alternative Modes on Pin			
				1	2	3	4
X1	28	ENET_RD2	GPIO1_IO28	ENET1_RGMII_RD2			
X1	29	ENET_TD3	GPIO1_IO18	ENET1_RGMII_TD3			
X1	30	ENET_RD3	GPIO1_IO29	ENET1_RGMII_RD3			
X1	31	ENET_TXC	GPIO1_IO23	ENET1_RGMII_TXC	ENET1_TX_ER		
X1	32	ENET_RXC	GPIO1_IO25	ENET1_RGMII_RXC	ENET1_RX_ER		
X1	33	ENET_TX_CTL	GPIO1_IO22	ENET1_RGMII_TX_CTL			
X1	34	GPIO1_IO00	GPIO1_IO00	CCM_ENET_PHY_REF_CLK_ROOT	CCM_EXT_CLK1	XTALOSC_REF_CLK_32K	
X1	35	ECSPI2_SCLK	GPIO5_IO10	UART4_RX (UART4_TX)	ECSPI2_SCLK		
X1	36	ENET_RX_CTL	GPIO1_IO24	ENET1_RGMII_RX_CTL			
X1	37	ECSPI2_MISO	GPIO5_IO12	UART4_CTS_B (UART4_RTS_B)	ECSPI2_MISO		
X1	38	ECSPI2_MOSI	GPIO5_IO11	UART4_TX (UART4_RX)	ECSPI2_MOSI		
X1	39	GND					
X1	40	GND					
X1	41	ECSPI1_SS0	GPIO5_IO09	UART3_RTS_B (UART3_CTS_B)	ECSPI1_SS0		
X1	42	ECSPI1_MOSI	GPIO5_IO07	UART3_TX (UART3_RX)	ECSPI1_MOSI		
X1	43	ECSPI2_SS0	GPIO5_IO13	UART4_RTS_B (UART4_CTS_B)	ECSPI2_SS0		
X1	44	ECSPI1_MISO	GPIO5_IO08	UART3_CTS_B (UART3_RTS_B)	ECSPI1_MISO		
X1	45	ECSPI1_SCLK	GPIO5_IO06	UART3_RX (UART3_TX)	ECSPI1_SCLK		
X1	46	UART4_TXD	GPIO5_IO29	UART4_TX (UART4_RX)	UART2_RTS_B (UART2_CTS_B)		
X1	47	GND					
X1	48	UART4_RXD	GPIO5_IO28	UART4_RX (UART4_TX)	UART2_CTS_B (UART2_RTS_B)	PCIE1_CLKREQ_B	
X1	49	UART2_TXD	GPIO5_IO25	UART2_TX (UART2_RX)	ECSPI3_SS0		
X1	50	UART1_RXD	GPIO5_IO22	UART1_RX (UART1_TX)	ECSPI3_SCLK		
X1	51	UART2_RXD	GPIO5_IO24	UART2_RX (UART2_TX)	ECSPI3_MISO		
X1	52	UART1_TXD	GPIO5_IO23	UART1_TX (UART1_RX)	ECSPI3_MOSI		
X1	53	I2C1_SDA	GPIO5_IO15	ENET1_MDIO	I2C1_SDA		
X1	54	UART3_RXD	GPIO5_IO26	USDHC3_RESET_B	UART3_RX (UART3_TX)	UART1_CTS_B (UART1_RTS_B)	
X1	55	I2C1_SCL	GPIO5_IO14	ENET1_MDC	I2C1_SCL		
X1	56	UART3_TXD	GPIO5_IO27	USDHC3_VSELECT	UART3_TX (UART3_RX)	UART1_RTS_B (UART1_CTS_B)	
X1	57	SAI3_MCLK	GPIO5_IO02	SAI3_MCLK	SAI5_MCLK	PWM4_OUT	
X1	58	GND					
X1	59	SAI3_TXC	GPIO5_IO00	SAI3_TX_BCLK	SAI5_RX_DATA2	UART2_TX (UART2_RX)	GPT1_COMPARE2
X1	60	SAI3_RXC	GPIO4_IO29	SAI3_RX_BCLK	SAI5_RX_BCLK	UART2_CTS_B (UART2_RTS_B)	GPT1_CLK
X1	61	SAI3_TXFS	GPIO4_IO31	SAI3_TX_SYNC	SAI5_RX_DATA1	SAI3_TX_DATA1	GPT1_CAPTURE2
X1	62	SAI3_RXFS	GPIO4_IO28	SAI3_RX_SYNC	SAI5_RX_SYNC	SAI3_RX_DATA1	GPT1_CAPTURE1
X1	63	SAI3_RXD	GPIO4_IO30	SAI3_RX_DATA0	SAI5_RX_DATA0	UART2_RTS_B (UART2_CTS_B)	GPT1_COMPARE1
X1	64	SAI3_TXD	GPIO5_IO01	SAI3_TX_DATA0	SAI5_RX_DATA3	GPT1_COMPARE3	
X1	65	SD2_WP	GPIO2_IO20	USDHC2_WP			
X1	66	SD2_CD_B	GPIO2_IO12	USDHC2_CD_B			
X1	67	SD2_RESET_B	GPIO2_IO19	USDHC2_RESET_B			
X1	68	GND					
X1	69	SD2_DATA0	GPIO2_IO15	USDHC2_DATA0			
X1	70	SD2_CMD	GPIO2_IO14	USDHC2_CMD			
X1	71	SD2_DATA1	GPIO2_IO16	USDHC2_DATA1			
X1	72	SD2_CLK	GPIO2_IO13	USDHC2_CLK			
X1	73	SD2_DATA2	GPIO2_IO17	USDHC2_DATA2			

X1: PIN 74 - 100

Con	Pin	Signal Name	GPIO Mode	Alternative Modes on Pin			
				1	2	3	4
X1	74	3V3					
X1	75	SD2_DATA3	GPIO2_IO18	USDHC2_DATA3			
X1	76	NVCC_SD2					
X1	77	GND					
X1	78	GND					
X1	79	JTAG_TRST_B		JTAG_TRST_B			
X1	80	JTAG_TDO		JTAG_TDO			
X1	81	JTAG_TCK		JTAG_TCK			
X1	82	JTAG_TDI		JTAG_TDI			
X1	83	JTAG_TMS		JTAG_TMS			
X1	84	SD1_RESET_B	GPIO2_IO10	USDHC1_RESET_B			
X1	85	SD1_CLK	GPIO2_IO00	USDHC1_CLK			
X1	86	SD1_STROBE	GPIO2_IO11	USDHC1_STROBE			
X1	87	SD1_CMD	GPIO2_IO01	USDHC1_CMD			
X1	88	GND					
X1	89	SD1_DATA0	GPIO2_IO02	USDHC1_DATA0			
X1	90	SD1_DATA4	GPIO2_IO06	USDHC1_DATA4			
X1	91	SD1_DATA1	GPIO2_IO03	USDHC1_DATA1			
X1	92	SD1_DATA5	GPIO2_IO07	USDHC1_DATA5			
X1	93	SD1_DATA2	GPIO2_IO04	USDHC1_DATA2			
X1	94	SD1_DATA6	GPIO2_IO08	USDHC1_DATA6			
X1	95	SD1_DATA3	GPIO2_IO05	USDHC1_DATA3			
X1	96	SD1_DATA7	GPIO2_IO09	USDHC1_DATA7			
X1	97	GND					
X1	98	GND					
X1	99	GND					
X1	100	GND					

©bytes at work

4.3 Carrier board connectors X2

X2: PIN 1 - 31

Con	Pin	Signal Name	GPIO Mode	Alternative Modes on Pin						
				1	2	3	4	5	6	7
X2	1	VSYS								
X2	2	VSYS								
X2	3	VSYS								
X2	4	VSYS								
X2	5	VSYS								
X2	6	VSYS								
X2	7	VSYS								
X2	8	VSYS								
X2	9	VSYS								
X2	10	VSYS								
X2	11	GND								
X2	12	GND								
X2	13	GND								
X2	14	GND								
X2	15	GND								
X2	16	GND								
X2	17	ONOFF		SNVS_ONOFF						
X2	18	GPIO1_IO01	GPIO1_IO01	PWM1_OUT	CCM_EXT_CLK2	XTALOSC_REF_CLK_24M				
X2	19	I2C4_SCL	GPIO5_IO20	PWM2_OUT	PCIE1_CLKREQ_B	I2C4_SCL				
X2	20	GPIO1_IO05	GPIO1_IO05	CCM_PMIC_READY	M4_NMI					
X2	21	I2C4_SDA	GPIO5_IO21	PWM1_OUT	I2C4_SDA					
X2	22	GPIO1_IO06	GPIO1_IO06	USDHC1_CD_B	ENET1_MDC	CCM_EXT_CLK3				
X2	23	MIPI_DSI_CLK_P		MIPI_DSI_CLK_P						
X2	24	GND								
X2	25	MIPI_DSI_CLK_N		MIPI_DSI_CLK_N						
X2	26	GPIO1_IO09	GPIO1_IO09	USDHC3_RESET_B	ENET1_1588_EVENT0_OUT	SDMA2_EXT_EVENT0				
X2	27	MIPI_DSI_D1_P		MIPI_DSI_D1_P						
X2	28	GPIO1_IO08	GPIO1_IO08	USDHC2_RESET_B	ENET1_1588_EVENT0_IN					
X2	29	MIPI_DSI_D1_N		MIPI_DSI_D1_N						
X2	30	GPIO1_IO07	GPIO1_IO07	USDHC1_WP	ENET1_MDIO	CCM_EXT_CLK4				
X2	31	MIPI_DSI_D0_P		MIPI_DSI_D0_P						

©bytesatwork

X2: PIN 32 - 66

Con	Pin	Signal Name	GPIO Mode	Alternative Modes on Pin						
				1	2	3	4	5	6	7
X2	32	GPIO1_IO15	GPIO1_IO15	USDHC3_WP	USB2_OTG_OC	PWM4_OUT	CCM_CLKO2	CCM_CLKO2	CCM_CLKO2	CCM_CLKO2
X2	33	MIPI_DSI_D0_N		MIPI_DSI_D0_N						
X2	34	GPIO1_IO14	GPIO1_IO14	USDHC3_CD_B	USB2_OTG_PWR	PWM3_OUT	CCM_CLKO1	CCM_CLKO1	CCM_CLKO1	CCM_CLKO1
X2	35	MIPI_DSI_D2_P		MIPI_DSI_D2_P						
X2	36	GPIO1_IO13	GPIO1_IO13	USB1_OTG_OC	PWM2_OUT					
X2	37	MIPI_DSI_D2_N		MIPI_DSI_D2_N						
X2	38	GPIO1_IO10	GPIO1_IO10	USB1_OTG_ID						
X2	39	MIPI_DSI_D3_P		MIPI_DSI_D3_P						
X2	40	GPIO1_IO11	GPIO1_IO11	USDHC3_VSELECT	USB2_OTG_ID	CCM_PMIC_READY				
X2	41	MIPI_DSI_D3_N		MIPI_DSI_D3_N						
X2	42	GPIO1_IO12	GPIO1_IO12	USB1_OTG_PWR	SDMA2_EXT_EVENT1					
X2	43	GND								
X2	44	GND								
X2	45	PCIE_RXN_P		PCIE1_RXN_P						
X2	46	SAI1_MCLK	GPIO4_IO20	SAI1_MCLK	SAI5_MCLK	SAI1_TX_BCLK	PDM_CLK			
X2	47	PCIE_RXN_N		PCIE1_RXN_N						
X2	48	SAI1_TXFS	GPIO4_IO10	SAI1_TX_SYNC	SAI5_TX_SYNC	ARM_PLATFORM_EVENTO				
X2	49	PCIE_TXN_P		PCIE1_TXN_P						
X2	50	SAI1_TXC	GPIO4_IO11	SAI1_TX_BCLK	SAI5_TX_BCLK	ARM_PLATFORM_EVENTI				
X2	51	PCIE_TXN_N		PCIE1_TXN_N						
X2	52	SAI1_TXD0	GPIO4_IO12	SAI1_TX_DATA0	SAI5_TX_DATA0	SRC_BOOT_CFG8	ARM_PLATFORM_TRACE8			
X2	53	PCIE_REF_PAD_CLK_P		PCIE1_REF_PAD_CLK_P						
X2	54	SAI1_TXD1	GPIO4_IO13	SAI1_TX_DATA1	SAI5_TX_DATA1	SRC_BOOT_CFG9	ARM_PLATFORM_TRACE9			
X2	55	PCIE_REF_PAD_CLK_N		PCIE1_REF_PAD_CLK_N						
X2	56	SAI1_TXD2	GPIO4_IO14	SAI1_TX_DATA2	SAI5_TX_DATA2	SRC_BOOT_CFG10	ARM_PLATFORM_TRACE10			
X2	57	GND								
X2	58	SAI1_TXD3	GPIO4_IO15	SAI1_TX_DATA3	SAI5_TX_DATA3	SRC_BOOT_CFG11	ARM_PLATFORM_TRACE11			
X2	59	MIPI_CSI_CLK_N		MIPI_CSI_CLK_N						
X2	60	SAI1_TXD4	GPIO4_IO16	SAI1_TX_DATA4	SAI6_RX_BCLK	SAI6_TX_BCLK	SRC_BOOT_CFG12	ARM_PLATFORM_TRACE12	ARM_PLATFORM_TRACE12	ARM_PLATFORM_TRACE12
X2	61	MIPI_CSI_CLK_P		MIPI_CSI_CLK_P						
X2	62	SAI1_TXD5	GPIO4_IO17	SAI1_TX_DATA5	SAI6_RX_DATA0	SAI6_TX_DATA0	SRC_BOOT_CFG13	ARM_PLATFORM_TRACE13	ARM_PLATFORM_TRACE13	ARM_PLATFORM_TRACE13
X2	63	MIPI_CSI_D0_N		MIPI_CSI_D0_N						
X2	64	SAI1_TXD6	GPIO4_IO18	SAI1_TX_DATA6	SAI6_RX_SYNC	SAI6_TX_SYNC	SRC_BOOT_CFG14	ARM_PLATFORM_TRACE14	ARM_PLATFORM_TRACE14	ARM_PLATFORM_TRACE14
X2	65	MIPI_CSI_D0_P		MIPI_CSI_D0_P						
X2	66	SAI1_TXD7	GPIO4_IO19	SAI1_TX_DATA7	SAI6_MCLK	SRC_BOOT_CFG15	ARM_PLATFORM_TRACE15	PDM_CLK	PDM_CLK	PDM_CLK

©bytesatwork

X2: PIN 67 - 100

Con	Pin	Signal Name	GPIO Mode	Alternative Modes on Pin						
				1	2	3	4	5	6	7
X2	67	MIPI_CSI_D1_N		MIPI_CSI_D1_N						
X2	68	SAI1_RXFS	GPIO4_IO00	SAI1_RX_SYNC	SAI5_RX_SYNC	ARM_PLATFORM_TRACE_CLK	SAI1_RX_SYNC			
X2	69	MIPI_CSI_D1_P		MIPI_CSI_D1_P						
X2	70	SAI1_RXC	GPIO4_IO01	SAI1_RX_BCLK	SAI5_RX_BCLK	ARM_PLATFORM_TRACE_CTL	SAI1_RX_BCLK			
X2	71	MIPI_CSI_D2_N		MIPI_CSI_D2_N						
X2	72	SAI1_RXD0	GPIO4_IO02	SAI1_RX_DATA0	SAI5_RX_DATA0	SAI1_TX_DATA1	SRC_BOOT_CFG0	ARM_PLATFORM_TRACE0	SAI1_RX_DATA0	PDM_BIT_STREAM0
X2	73	MIPI_CSI_D2_P		MIPI_CSI_D2_P						
X2	74	SAI1_RXD1	GPIO4_IO03	SAI1_RX_DATA1	SAI5_RX_DATA1	SRC_BOOT_CFG1	ARM_PLATFORM_TRACE1	PDM_BIT_STREAM1		
X2	75	MIPI_CSI_D3_N		MIPI_CSI_D3_N						
X2	76	GND								
X2	77	MIPI_CSI_D3_P		MIPI_CSI_D3_P						
X2	78	SAI1_RXD2	GPIO4_IO04	SAI1_RX_DATA2	SAI5_RX_DATA2	SRC_BOOT_CFG2	ARM_PLATFORM_TRACE2	PDM_BIT_STREAM2		
X2	79	GND								
X2	80	SAI1_RXD3	GPIO4_IO05	SAI1_RX_DATA3	SAI5_RX_DATA3	SRC_BOOT_CFG3	ARM_PLATFORM_TRACE3	PDM_BIT_STREAM3		
X2	81	SAI2_MCLK	GPIO4_IO27	SAI2_MCLK	SAI5_MCLK					
X2	82	SAI1_RXD4	GPIO4_IO06	SAI1_RX_DATA4	SAI6_TX_BCLK	SAI6_RX_BCLK	SRC_BOOT_CFG4	ARM_PLATFORM_TRACE4		
X2	83	SAI2_TXFS	GPIO4_IO24	UART1_CTS_B (UART1_RTS_B)						
X2	84	SAI1_RXD5	GPIO4_IO07	SRC_BOOT_CFG5	ARM_PLATFORM_TRACE5					
X2	85	SAI2_TXC	GPIO4_IO25							
X2	86	SAI1_RXD6	GPIO4_IO08	SRC_BOOT_CFG6	ARM_PLATFORM_TRACE6					
X2	87	SAI2_TXD0	GPIO4_IO26							
X2	88	SAI1_RXD7	GPIO4_IO09	SRC_BOOT_CFG7	ARM_PLATFORM_TRACE7					
X2	89	SAI2_RXFS	GPIO4_IO21	UART1_TX (UART1_RX)						
X2	90	SAI5_MCLK	GPIO3_IO25							
X2	91	SAI2_RXC	GPIO4_IO22	UART1_RX (UART1_TX)						
X2	92	SAI5_RXFS	GPIO3_IO19							
X2	93	SAI2_RXD0	GPIO4_IO23	UART1_RTS_B (UART1_CTS_B)						
X2	94	SAI5_RXC	GPIO3_IO20	PDM_CLK						
X2	95	SAI5_RXD2	GPIO3_IO23	PDM_BIT_STREAM2						
X2	96	SAI5_RXD0	GPIO3_IO21	PDM_BIT_STREAM0						
X2	97	SAI5_RXD3	GPIO3_IO24	PDM_BIT_STREAM3						
X2	98	SAI5_RXD1	GPIO3_IO22	PDM_BIT_STREAM1						
X2	99	GND								
X2	100	GND								

©bytesatwork

4.4 Power Supply

> The byteENGINE can be powered with 3.6V to 5.5V.
> The recommended power supply is 5V.

LINK:
PCA9450AAHNY Power Manage IC (PMIC) for i.MX 8M Mini

4.5 Boot Modes byteENGINE IMX8MM

The Module is designed to boot from SDCARD. If a valid u-boot is placed in NOR Flash it will boot from NOR. If a valid u-boot is present on SDCARD it always boots from SDCARD regardless of the content of the NOR Flash.
The boot sequence can be redefined with OPT flashing.

LINK:
Datasheet of NXP i.MX 8M Mini

5. Ordering Info

The Order Code allows customers to easily recognize the detailed specification of the ordered SOM.
Please refer to chapter **„3.4 Additional information“ on page 7** for further information concerning the CPU.

	[SOM]-byteENGINE-IMX8MM-[TYPE]-[SPEED]-[RAM]-[FLASH]-[temp range]-[revision]	
[SOM]:	SOM type	bE: byteENGINE
IMX8MM-[TYPE]	CPU type	IMX8MM-QUAD, IMX8MM-DUAL, IMX8MM-QUADLITE
[SPEED MHz]:	Clock speed	1.6 GHz, 1.8 GHz
R[xxx MB]:	RAM size	256, 512, 1024, 1536, 2048, 4096 MB
[E/GB]:	eMMC flash size	4, 8, 16, 32, 64 GB
[C, I]:	Temperature range	[C] Customer 0° to +95° Celsius, [I] Industrial -40° to +85° Celsius

Example: byteENGINE-IMX8MM-QUAD-1600-R512-E8-i

©bytes at work

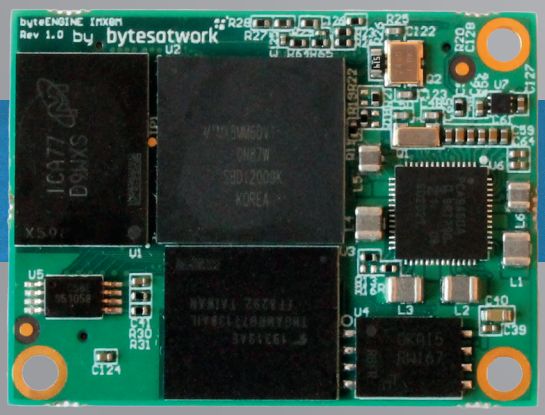
6. References

NOTICE
Files can only be downloaded with login credentials.
Please request your download credentials via
info@bytesatwork.ch or contact your sales representative.

LINKS:

>	Schematic of the connectors X1 and X2	Chapter: 3.7
>	Altium schematic of connectors X1 and X2	Chapter: 3.7
>	Altium Library	
>	STEP Model	
>	Detailed pinout for byteENGINE IMX8MM	Chapter: 4.2, 4.3
>	Datasheet of Neltron 2001S-100G-270-020 Connectors	Chapter: 3.8
>	NXP i.MX 8M Mini Family	Chapter: 3.2, 3.4
>	PCA9450AAHN Power Manage IC (PMIC) for i.MX8M Mini	Chapter: 4.4
>	Datasheet of NXP i.MX 8M Mini	Chapter: 4.5
>	NXP Config Tools for i.MX Applications Processors	Chapter: 3.10
>	byteENGINE IMX8MM config file for config tools	Chapter: 3.10
>	meta-bytesatwork on github	Chapter: 3.2
>	byteWIKI	

7. Contact information



- bytes at work AG
  Technoparkstrasse 7
  CH-8406 Winterthur
  Switzerland
- Phone: +41 52 213 79 79
  Fax: +41 52 203 27 13
- eMail: info@bytesatwork.ch
- Product Information:
  www.bytesatwork.io
- Help:
  www.bytesatwork.io/support

bytesatwork